

## CLAIMS

1. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first PMOS device and a first NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second PMOS device with a drain connected to an effective ground terminal and with a source connected to a source of the first NMOS device.

2. The integrated circuit of claim 1 wherein,

the second NMOS device is a **depletion** transistor; and

the second PMOS device is a **depletion** transistor.

3. The integrated circuit of claim 1 wherein,

the first PMOS device is an **ordinary enhancement** transistor;

the first NMOS device is an **ordinary enhancement** transistor;

the second NMOS device is a **depletion** transistor; and

the second PMOS device is a **depletion** transistor.

4. The integrated circuit of claim 1 wherein,

the first PMOS device is a low threshold voltage **ordinary enhancement** transistor;

the first NMOS device is a low threshold voltage **ordinary enhancement** transistor;

- the second NMOS device is a **depletion** transistor; and
- the second PMOS device is a **depletion** transistor.
5. The integrated circuit of claim 1 wherein,
- the second NMOS device is a **leaky enhancement** transistor; and
- the second PMOS device is a **leaky enhancement** transistor.
6. The integrated circuit of claim 1 wherein,
- the first PMOS device is an **ordinary enhancement** transistor;
- the first NMOS device is an **ordinary enhancement** transistor;
- the second NMOS device is a **leaky enhancement** transistor; and
- the second PMOS device is a **leaky enhancement** transistor.
7. The integrated circuit of claim 1 wherein,
- the first PMOS device is a low threshold voltage **ordinary enhancement** transistor;
- the first NMOS device is a low threshold voltage **ordinary enhancement** transistor;
- the second NMOS device is a **leaky enhancement** transistor; and
- the second PMOS device is a **leaky enhancement** transistor.
8. The integrated circuit of claim 1 further including:
- a first logic input to a gate of the first PMOS device; and
- a second logic input to a gate of the first NMOS device.
9. The integrated circuit of claim 1 further including:
- a logic input to a gate of the first PMOS device and to a gate of the first NMOS device.

10. The integrated circuit of claim 1 further including:

a first logic input to a gate of the first PMOS device;

a second logic input to a gate of the first NMOS device;

a first control input to a gate of the second NMOS device; and

a first control input to a gate of the second PMOS device.

11. The integrated circuit of claim 1 further including:

at least one control input to the multi-state circuit connected to control the state of the multi-state circuit when the second NMOS device and the second PMOS device are turned on;

respective control inputs to the respective second NMOS device and to the second PMOS device connected to control turn on and turn off of the second NMOS device and the second PMOS device so as to turn them on together and to turn them off together;

whereby the at least one control input to the multi-state circuit does not effect changes in state of the multi-state circuit when the second NMOS device and the second PMOS device are turned off.

12. The integrated circuit of claim 1 further including:

a pull-up sustaining NMOS device with a with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining PMOS device with a with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

13. The integrated circuit of claim 1 wherein,

the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first

PMOS device such that the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off. **(IS THIS CLAIM OK?)**

14. The integrated circuit of claim 1 wherein,

the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off. **(IS THIS CLAIM OK?)**

15. The integrated circuit of claim 1 wherein,

the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; and

the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off. **(IS THIS CLAIM OK?)**

16. The integrated circuit of claim 1 wherein,

the multi-state circuit includes multiple first PMOS devices, and further including;

one or more second NMOS device having a source connected to respective sources of one or more of the multiple first PMOS devices.

17. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off

and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second **depletion or leaky enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **depletion or leaky enhancement** PMOS device with a drain connected to an effective ground terminal and with a source connected to a source of the first NMOS device;

wherein the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; and

wherein the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off.

18. The integrated circuit of claim 17 further including:

a pull-up sustaining **depletion or leaky enhancement** NMOS device with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining **depletion or leaky enhancement** PMOS device with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

19. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off

and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device;

wherein the first PMOS device and the second NMOS device are sized relative to each other so that a channel conduction of the second NMOS device is sufficiently less than that of the first PMOS device such that the second NMOS device becomes reverse biased when the multi-state circuit is in the second state and second NMOS device is turned off; and

wherein the first NMOS device and the second PMOS device are sized relative to each other so that a channel conduction of the second PMOS device is sufficiently less than that of the first NMOS device such that the second PMOS device becomes reverse biased when the multi-state circuit is in the first state and second PMOS device is turned off.

20. The integrated circuit of claims 19 further including:

a pull-up sustaining **ordinary enhancement** NMOS device with a with a drain connected to the supply voltage terminal and with a source connected to a source of the first PMOS device and with a gate connected to an output node of the multi-state circuit; and

a pull-down sustaining **ordinary enhancement** PMOS device with a with a drain connected to the effective ground terminal and with a source connected to the source of the first NMOS device and with a gate connected to the output node of the multi-state circuit.

21. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first PMOS device and a first NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device

is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device.

22. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **ordinary enhancement** PMOS device and a first **ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device.

23. An integrated circuit for use with a supply voltage and an effective ground voltage, comprising:

a multi-state circuit that includes a first **low threshold ordinary enhancement** PMOS device and a first **low threshold ordinary enhancement** NMOS device, the multi-state circuit being operable to switch between a first state in which the first PMOS device is turned on and the first NMOS device is turned off and a second state in which the first PMOS device is turned off and the first NMOS device is turned on;

a second **ordinary enhancement** NMOS device with a drain connected to a supply voltage terminal and with a source connected to a source of the first PMOS device; and

a second **ordinary enhancement** PMOS device with a drain connected to a an effective ground terminal and with a source connected to a source of the first NMOS device.

24. A method of limiting power consumption during operation of the circuit of claim 21, 22 or 23 comprising:

reducing leakage current through the first NMOS device while the multi-state circuit is in the first state by causing a reverse biasing of the second PMOS device and the first NMOS device; and

reducing leakage current through the first PMOS device when the multi-state circuit is in the second state by causing a reverse biasing of the second NMOS device and the first PMOS device.

25. A method of limiting power consumption during operation of the circuit of claim 21, 22 or 23 comprising:

in the active mode,

providing a turn on voltage signal to a gate of the second NMOS device that is higher than the multi-state circuit supply voltage bias; and

providing a turn on voltage signal to a gate of the second PMOS device that is lower than the multi-state circuit effective ground bias voltage; and

in a standby mode,

providing a turn off voltage signal to a gate of the second NMOS device that is not as low as the turn on voltage signal provided to the gate of the second PMOS device in the active mode; and

providing a turn off voltage signal to a gate of the second PMOS device that is not as high as the turn on voltage signal provided to the gate of the second NMOS device in the active mode.

26. A method of limiting power consumption during operation of the circuit of claim 21, 22 or 23 comprising:

in the active mode,

providing a turn on voltage signal to a gate of the second NMOS device that is higher than the multi-state circuit supply voltage bias; and

providing a turn on voltage signal to a gate of the second PMOS device that is lower than the multi-state circuit effective ground bias voltage; and

in a standby mode,

providing a turn off voltage signal to a gate of the second NMOS device that is equal to the multi-state circuit effective ground bias voltage; and

providing a turn off voltage signal to a gate of the second PMOS device that is equal to the multi-state circuit supply voltage bias.

27. A method of limiting power consumption during operation of the circuit of claim 21, 22 or 23 comprising:

in the active mode,

providing high enough turn on voltage signal to a gate of the second NMOS device while providing a low enough turn on voltage signal to a gate of the second PMOS to drive current sufficient to achieve a substantially full voltage swing whenever the multi-state circuit changes states in the active mode; and

in a standby mode,

providing a turn off voltage signal to the gate of the second NMOS device that is higher than the turn on voltage provided to the gate of the PMOS device in the active mode while providing a turn off voltage signal to the gate of the second PMOS device that is lower than the turn on voltage provided to the gate of the NMOS device in the active mode.

28. A method of limiting power consumption during operation of the circuit of claim 21, 22 or 23 comprising:

in the active mode,

providing high enough turn on voltage signal to a gate of the second NMOS device while providing a low enough turn on voltage signal to a gate of the second PMOS to drive current sufficient to achieve a substantially full voltage swing whenever the multi-state circuit changes states in the active mode; and

in a standby mode,

providing a turn off voltage signal to the gate of the second NMOS device that is equal to the multi-state circuit effective ground bias voltage while providing a turn off voltage signal to the gate of the second PMOS device that is equal to the multi-state circuit supply voltage bias.

29. An integrated circuit for use with a supply voltage and an effective ground voltage comprising:

an **enhancement** NMOS transistor with a drain connected to a supply voltage terminal; and

a multi-state circuit connected to a source of the NMOS transistor and connected to an effective ground terminal.

30. An integrated circuit for use with a supply voltage and an effective ground voltage comprising:

an **enhancement** PMOS transistor with a drain connected to an effective ground voltage terminal; and

a multi-state circuit connected to a supply voltage terminal and connected to a source of the PMOS transistor.

31. An integrated circuit for use with a supply voltage and an effective ground voltage comprising:

an **enhancement** NMOS transistor with a drain connected to a supply voltage terminal;

an **enhancement** PMOS transistor with a drain connected to an effective ground voltage terminal; and

a multi-state circuit connected to a source of the NMOS transistor and connected to source of the PMOS transistor.

32. A method of limiting power consumption during operation of the circuit of claim 29 comprising:

in the active mode,

providing a turn on voltage signal to a gate of the NMOS transistor that is higher than a supply voltage; and

in a standby mode,

providing a turn off voltage signal to a gate of the NMOS transistor that is lower than the supply voltage.

33. A method of limiting power consumption during operation of the circuit of claim 30 in active mode comprising:

inactive mode,

providing a turn on voltage signal to a gate of the PMOS transistor that is lower than the effective ground voltage; and

in a standby mode,

providing a turn off voltage signal to a gate of the PMOS transistor that is higher than the effective ground voltage.

34. A method of limiting power consumption during operation of the circuit of claim 31 comprising:

in the active mode,

providing a turn on voltage signal to a gate of the NMOS transistor that is higher than a supply voltage; and

providing a turn on voltage signal to a gate of the PMOS transistor that is lower than the effective ground voltage; and

in a standby mode,

providing a turn off voltage signal to a gate of the NMOS transistor that is not lower than the effective ground voltage; and

providing a turn off voltage signal to a gate of the PMOS transistor that is not higher than the supply voltage.